

# Optical FET receivers for neural network applications

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## ABSTRACT

Optical FET detectors were fabricated in both the MOSIS/Vitesse HGaAs3 process and the AT&T field-effect-transistor-self-electrooptic effect device (FET-SEED) process.<sup>1</sup> Typical responsivity is in the order of 1,000A/W and response time in the order of 10 to 100  $\mu$ sec at 50nW optical input power. Such high gain detectors through commercially available industrial foundries are especially useful for optical neural network applications where high density integration requires very good uniformity and power dissipation limits the available optical power. The mechanism of such optical FET detectors are discussed.

**Keywords:** photodetectors, GaAs MESFETs, FET-SEEDs, optical neural networks, smart pixels

## 1 INTRODUCTION

The optical implementation of a neural network usually consists of two-dimensional neuron arrays that are interconnected via the third dimension. Optoelectronic circuits provide a useful tool for the fabrication of optical neuron arrays due to its capability of implementing complex neuron response functions. The basic optoelectronic circuit in a neuron array consists of one or more photodetectors, FETs, and optical output devices. The optical signal received on its photodetectors is mapped to its output intensity through the FET circuits. By implementing the I/O process optically rather than electrically, one can achieve parallel processing and greatly reduce the number of pins on a chip.

A high density neuron array requires photodetectors with high gain.<sup>2</sup> Because of the high loss involved in optical interconnections, the optoelectronic circuit must provide optical gain in addition to performing the desired response function in order to make multilayer cascade networks possible. Due to the electrical power dissipation limit on a certain chip, the optical output power from a neuron circuit is usually limited. After the high loss interconnections, a high gain photodetector is necessary in order to perform the desired computation. If the photodetector does not provide enough gain, additional stages of amplification will be needed, thus increasing the area per pixel and decreasing the neuron density. Another disadvantage of low efficiency photodetectors is the reduced switching speed when the detector can not provide strong enough switching current.

A critical issue for large scale integration of high density neuron circuits is the non-uniformity due to fabrication

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imperfections. Poor uniformity among neuron circuits requires a higher level of optical power, therefore increases the power dissipation and reduces the achievable array density. Due to the high sensitivity of FETs to process variations, it is desirable to use a well-established process for the fabrication of high density neuron arrays in order to achieve better uniformity. Therefore, industrial foundries are preferred for the fabrication of VLSI optoelectronic arrays.

Because one can monolithically integrate optical output devices, such as light-emitting-diodes (LEDs), laser diodes, or optical modulators, with photodetectors and metal-semiconductor-FET (MESFET) circuitry, GaAs is an excellent material for fabricating high density optoelectronic neuron arrays. However, most of the GaAs industrial foundries do not have a complementary process that is required for the fabrication of high gain bipolar photo transistors. Only high speed metal-semiconductor-metal (MSM) detectors are available. Unfortunately, its low responsivity (0.01-0.1A/W) is too low for high density arrays. In this paper, we report the result of using MESFETs as high gain photodetectors. These FETs are fabricated by two available foundries: Vitesse Semiconductor Corp. HGaAs3 process through MOSIS<sup>3</sup> and AT&T FET-SEED process through the FET-SEED workshop organized by the Consortium for Optical and Optoelectronic Technologies for Computing (CO-OP).<sup>4</sup> These optical FET (OPFET) detectors have very high gain at low optical input power, typically in the order of 1,000A/W for 50nW input, and moderate speed. It is therefore suitable for neural network applications. In the following, we will report the experimental result on the responsivity and response time of OPFET detectors. Possible mechanism will be discussed.

## 2 OPFET FROM MOSIS/VITESSE HGAAS3 PROCESS

### 2.1 Fabrication process

Vitesse Semiconductor Corp. provides low cost custom designed GaAs MESFET integrated circuits through MOSIS. The HGaAs3 process offers enhancement-mode and depletion-mode GaAs MESFETs (EFET and DFET) with 0.8 $\mu$ m minimum feature size and four levels of Aluminum interconnect metalization. The MESFETs are fabricated by Si n<sup>-</sup> ion implant on the surface of semi-insulating GaAs substrates with slightly p-doped ion implant. The gate metal is then deposited and used as a mask for the self-aligned source and drain n<sup>+</sup> ion implant (Figure 1). Good uniformity is achieved using this process.<sup>5</sup> Furthermore, because Vitesse uses refractory metals for the Schottky and ohmic contacts, these electronic circuits can withstand temperatures up to 530°C for several hours without significant degradation in performance. Therefore, it is possible to regrow heterostructures on such circuits to integrate optical devices using low temperature molecular-beam-epitaxy (MBE).<sup>6</sup> Different kinds of light sources, such as LEDs,<sup>5</sup> laser diodes, and multiple-quantum-well (MQW) modulators can be grown using this method, thus allowing the fabrication of complex optoelectronic circuits and arrays.

As mentioned earlier, MSM detectors have very low efficiency and therefore are not a good choice for large optoelectronic neuron arrays. As a result, we investigated the possibility of using EFETs as photodetectors. The EFET has a threshold voltage of -0.65V and low dark currents, typically in the order of 10nA for an EFET with 10 $\mu$ m gate width. Its cross section is shown in Figure 1. The depth of the n channel and the n<sup>+</sup> implant are 0.3 $\mu$ m and 0.6 $\mu$ m, respectively. In order to absorb the incoming photons, the ohmic metal contacts on the source and drain do not extend completely to the gate region.

### 2.2 I-V characteristics and responsivity results

Figure 2 shows the I-V characteristics of an OPFET under different illumination powers from a laser diode ( $\lambda = 837$ nm) when its gate was left floating. The EFET had a gate width of 40 $\mu$ m and a gate length of 1 $\mu$ m with a spacing of 8 $\mu$ m between the gate and the ohmic contacts while the focused laser beam has a diameter of about

30 to 40  $\mu\text{m}$ . The dark current of this FET was 10nA. By using a serpentine gate design, we can increase the photon absorption area, and therefore increase the detector gain. However, the dark current is also increased. In Figure 2 we also plotted the IV curves when different gate voltages were applied under dark conditions. Notice how the response due to the optical signal is similar to the response due to the applied electrical gate bias. Thus, one can think of the OPFETs as having an optical gate. The conductance of the channel is modulated by the optical input power. With only 10nW optical input, the OPFET drain-source current is more than 20 $\mu\text{A}$ , which corresponds to a responsivity of more than 2,000A/W.

The detector drain-source saturation current is plotted in Figure 3 as a function of the optical input power on a log-log scale. For the upper curve the gate was left floating while for the lower curve the gate was shorted to the source ( $V_{gs} = 0\text{V}$ ). We observed a square-root dependence of the drain-source current on the optical input power. The OPFET responsivity is not constant but decreases as input power increases. It changed from about 2,000A/W at 10nW input to 200A/W at 1 $\mu\text{W}$  input. Notice that when the gate-source voltage was clamped, the responsivity was greatly reduced by two orders of magnitude.

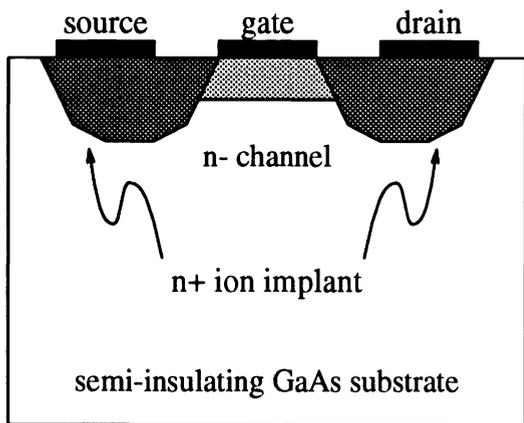


Figure 1. Cross section of the MOSIS enhancement-mode FET. The substrate is slightly p doped.

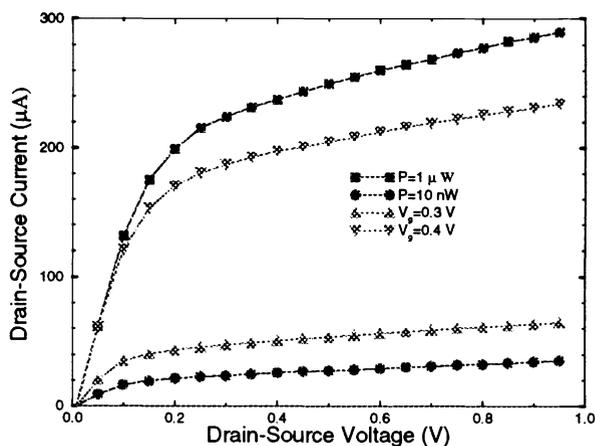


Figure 2. I-V characteristics of a MOSIS OPFET with different optical and electrical inputs. Its dark current is 10nA.

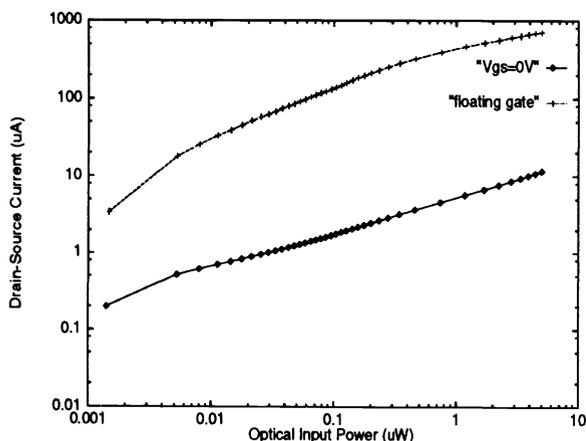


Figure 3. OPFET responsivity with the gate floating and the gate tied to the source. Plotted in log scale.

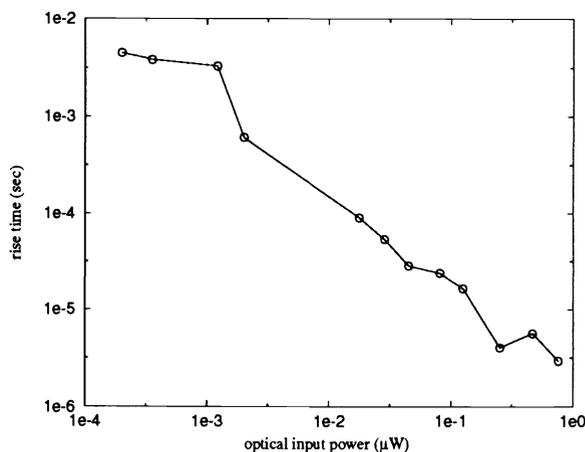


Figure 4. OPFET response time with gate floating. Square-wave optical signal was used for the measurement.

## 2.3 Response time measurement

The time response of gate-floating OPFETs was measured by illuminating the gate region with a square-wave optical signal. This signal changes from zero input to variable high levels. We observed a roughly symmetric rise and fall response. Figure 4 shows the measured 10At 22nW average input, a rise time of 25 $\mu$ sec was measured. The OPFET bandwidth shows a roughly linear dependence on the optical input power.

## 2.4 Discussion on OPFET mechanism

The response of ion-implanted GaAs MESFET to optical illumination has been studied extensively.<sup>7-9</sup> The main mechanism responsible for the photosensitivity of the MESFETs is due to the deep-level traps in the substrate. Figure 2 and the observation that the responsivity of OPFETs is linearly proportional to the EFET gate width/length ratio suggest a strong relation between the high gain OPFET and the MESFET operation mechanism. As mentioned in the previous section, one can think of the OPFET as having an optical gate. When the gate is left floating, the photon-generated carriers produce a forward voltage across the gate-channel Schottky diode, which is equivalent to applying a positive voltage on the gate. As a result, the channel conductance is greatly increased and high responsivity is achieved. Even with the gate tied to the source, because the substrate is slightly p-doped, a substrate-channel depletion region is formed on the interface and the substrate acts as a backgate. The modulation of this depletion region (or backgate voltage) by photon-generated carriers will also change the conductance of the channel. However, its responsivity is not as high as when the gate is floating because the substrate-channel depletion region is much wider than the gate-channel depletion region.

# 3 OPFET FROM FET-SEED PROCESS

The integration of GaAs/AlGaAs FET and SEEDs in a batch fabrication process<sup>1</sup> has been applied to the fabrication of optoelectronic smart pixels<sup>10-12</sup> and other applications.<sup>13</sup> It provides the advantage of monolithically integrating FET circuitry and multiple-quantum-well (MQW) SEEDs in a single fabrication process. Therefore, no post-processing is required for optoelectronic neuron array fabrication as compared to the case of MBE regrowth on MOSIS GaAs circuits. MQW SEEDs/photodiodes have been used as photodetectors on this process.<sup>1,10-13</sup> Unlike the HGaAs3 process, only enhancement-mode FETs are available here, thus it puts some limits on the circuit design and performance. Similar to MSM detectors, MQW photodiodes have high speed (GHz) but low responsivity (less than 0.7A/W). In the following, we report the successful demonstration of using the FETs by AT&T FET-SEED process as a high gain OPFET suitable for neuron array applications. These detectors have a responsivity as high as 10,000A/W and a fall time on the order of 10 $\mu$ sec at 20nW optical input power. The dark current is controlled by bias gate voltages and can be below 1nA.

## 3.1 Structure and fabrication

The FET structure is schematically shown in Figure 5. Detailed description was given by T. K. Woodward et al.<sup>10</sup> The channel consists of a 100 $\text{\AA}$  n-doped GaAs conducting layer and a 900 $\text{\AA}$  AlGaAs undoped spacer located between the gate electrode and the channel. The source and drain contacts are made to the channel through ohmic contacts which penetrate from the top n+ GaAs layer to the n-channel layer. Under the channel, there are a multiple-quantum-well (MQW) region and a p+ conducting layer. The p+ layer is electrically addressable by Be ion implantation, which acts as a backgate to the FET. As we will see later, similar to the case of MOSIS OPFETs, this backgate plays a very important role in the operation of the OPFET. The FET has a gate width of 10 $\mu$ m and a length of 1 $\mu$ m, with a spacing of 2 $\mu$ m between the gate and the ohmic contacts. The FET-SEED

process provides EFETs only, where the threshold voltage is typically  $-1.2\text{V}$ . Their source-drain conductance can be controlled electrically by applying a voltage to either the gate or backgate.

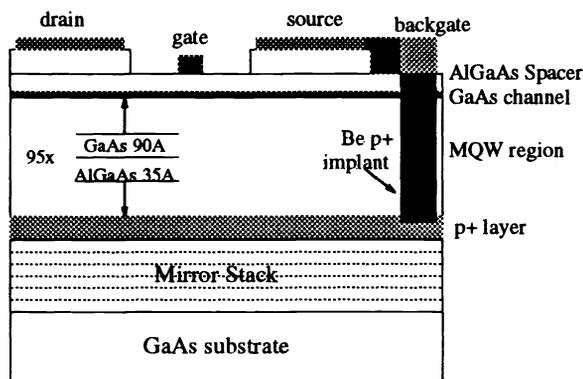


Figure 5. Cross-section of the FET. The MQW region under the  $n+$  channel is designed for modulator/SEED, and can be used as the absorption layer for photodetectors.

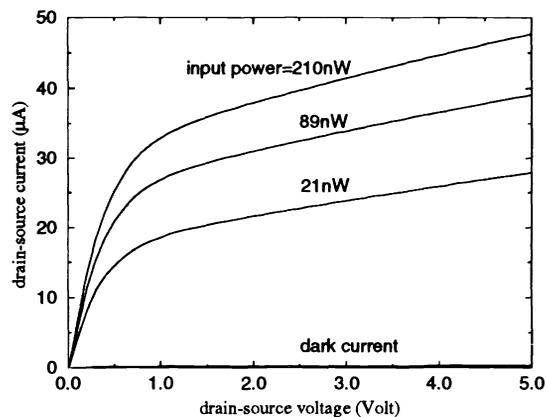


Figure 6. I-V characteristics of the OPFET. Gate voltage is fixed at  $-1.5\text{V}$ , while the backgate is floating. The dark current is  $0.20\mu\text{A}$  at  $V_{ds}=2.5\text{V}$ .

### 3.2 Responsivity results

In order to use this FET as a photodetector, we had to bias either the gate or the backgate to the subthreshold regime so that the dark current is low, typically below  $1\text{nA}$ . By shining light on the FET gate region, we observed a dramatic increase in the channel current, as shown in Figure 6. Due to different designs, these FETs have higher saturation voltages compared to MOSIS FETs.

From this I-V curve, we calculated the responsivity of the FET detector by simply dividing the photocurrent by the optical input power. For  $21\text{nW}$  optical input, we measure a photocurrent of more than  $21\mu\text{A}$  at  $V_{ds} = 2.5\text{V}$ , which gives us a responsivity of over  $1,000\text{A/W}$ . The focused light spot is much larger than the gate region — the focused spot is estimated to have a diameter of  $30\mu\text{m}$  to  $40\mu\text{m}$  while the gate opening is only  $4 \times 10\mu\text{m}^2$  — and therefore most of the light is wasted outside the gate region. Thus, the actual detector gain can be about an order of magnitude higher if the illuminating light is focused to a smaller spot. This can be achieved by using better light source and focus optics or increasing the gate opening area using interdigital gate geometry as we previously demonstrated with GaAs OPFETs fabricated through MOSIS.

Figure 7 shows the responsivity of the OPFET under different gate bias voltages with the backgate contact floating. We get a high gain when the optical input power is low, typically in the order of  $1,000\text{A/W}$  for input power lower than  $50\text{nW}$ . An interesting phenomena is that the OPFET responsivity does not depend much on the dark current. With the dark current reduced from  $0.20\mu\text{A}$  to  $0.23\text{nA}$ , the responsivity only reduced by a factor of 1.6.

### 3.3 Mechanism

The mechanism here is different from that of the MOSIS OPFET. Since the conducting layer of the FET is so thin (only  $100\text{\AA}$ ), it is basically transparent to the optical input signal. Therefore, the absorption must happen

in the MQW region underneath. We verified this by measuring the spectral responses of the optical FET and the MQW photodiode. The two spectral responses have almost identical exciton peaks and absorption edges.

When light is absorbed in the MQW region, electron-hole pairs are generated. Under the built-in electric field, holes are swept into the backgate layer while electrons go to n-channel. In the case where the gate voltage is fixed and the backgate is floating, the accumulation of holes in the backgate region charges up its voltage just as a p-i-n photodiode. As a result, the positive voltage that builds up on the backgate contact increases the conductance of the FET dramatically. The measured photo-induced positive voltage on the backgate is very similar to that of a typical photodiode. When the input power is low, we observe a sharp increase in the backgate voltage, which gives very high responsivity. As  $P_{in}$  becomes stronger, the backgate voltage grows logarithmically. In return, the responsivity decreases to below 500A/W. Based on the photo-induced backgate voltage measurement and the measured backgate transconductance, we calculated the expected photocurrent. The result agreed with our experimental measurement.

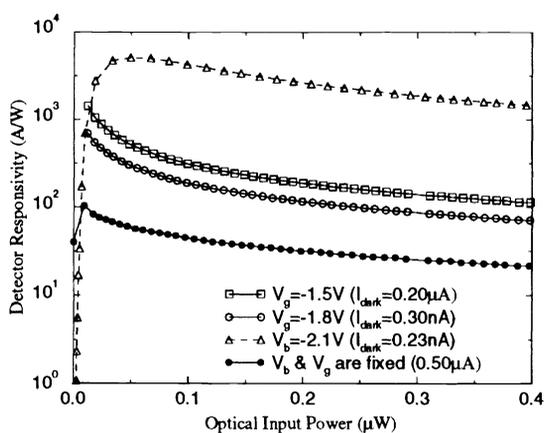


Figure 7. Responsivity of the optical FET with the backgate or the gate floating. Solid curves are plotted for different gate voltages with the backgate floating. The dashed curve is with the gate floating. In comparison is the filled curve when both gate and backgate voltages are fixed.

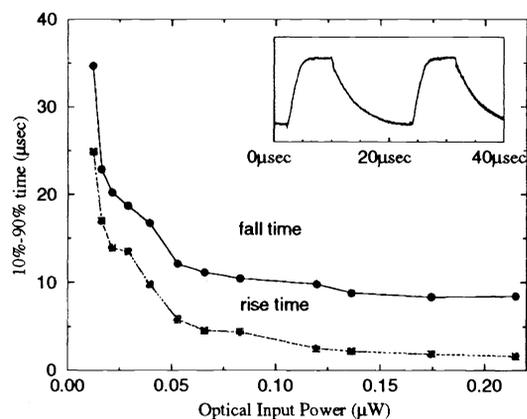


Figure 8. Time response of the optical FET with the backgate floating. Gate voltage is fixed at  $-1.8V$ , which gives a dark current of  $0.30nA$ .

This optical FET can also be operated with the gate floating while the dark current is controlled by backgate bias. The mechanism is slightly different. Since the backgate is now electrically connected, photo-generated holes will be swept away while electrons are trapped at the n-channel. In order to maintain charge neutrality, we believe positive charges are generated at the gate contact through surface states. As a result, the gate-voltage increases and increased photocurrent is observed. Figure 7 also shows the measured result for this mode. Again, the FET detector has high gain but with different behavior. We observe a peak in the responsivity curve which is attributed to the peak of FET transconductance when plotted as a function of gate voltage.<sup>11</sup> Measuring the photo-induced gate voltage, we calculated the expected photocurrent and again it agreed well with experiment measurement. If both the gate and the backgate voltages are fixed, this photo-induced gate/backgate voltage mechanism is no longer valid, and the detector gain is low as we can see from Figure 3. However, it still a gain as high as 50A/W, which may be attributed to the photoconductance effect.

### 3.4 Response time

We measured the response time of these OPFETs with the method we described earlier. However, we observed asymmetric rise and fall responses: the rise time is faster than the fall time. The exact reason for this behavior is yet not clear. Figure 8 shows the measured result as a function of signal high level. We can estimate the expected rise time as

$$\Delta t \simeq \frac{C\Delta V}{I}$$

where  $C$  is the capacitance of the  $i$ -MQW region,  $\Delta V$  is the voltage swing on the backgate, and  $I$  is the photo-generated charging current. For 215nW optical input power, if we use  $30\mu\text{m}$  as the diameter of the focus spot, only 12.2nW power is absorbed in the MQW region through the  $4 \times 10\mu\text{m}^2$  window on the surface, which gives us a charging current of 4.88nA assuming the efficiency of the MQW photodiode is 0.4A/W. The total area under the FET is  $16 \times 10\mu\text{m}^2$ , giving us a capacitance of 16.2fF. From our measurement, the generated voltage swing is 0.56V for  $P_{in}=215\text{nW}$ . Based on these numbers, we can calculate the rise time to be  $1.87\mu\text{sec}$ , which is very close to our measured  $1.65\mu\text{sec}$  result.

When operated with the gate floating, the OPFET shows longer response time, in the order of  $100\mu\text{sec}$ , most likely because surface states are involved when operating in this mode.

## 4 SUMMARY

We were able to use the FETs from the MOSIS/Vitesse HGaAs3 process and the AT&T FET-SEED process as a high responsivity detector. The OPFET has very high responsivity at low optical input, typically in the order of 1,000A/W or higher. With the 10 to  $100\mu\text{sec}$  response time, it is suitable for applications on optical neural network. We attributed such high gain to the modulation of gate/backgate voltage by photo-generated carriers near the channel. The deduced result based on this model agreed well with our experimental measurement.

## 5 ACKNOWLEDGMENTS

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